650V GaN Power Transistor (FET)

Features

- Easy to use, compatible with standard gate drivers
- Excellent Q_G x $R_{DS(on)}$ figure of merit (FOM)
- Low Q_{RR}, no free-wheeling diode required
- Low switching loss
- RoHS compliant and Halogen-free

Product Summary

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V_{DSS}	650	V
$R_{DS(on), typ}$	120	mΩ
$Q_{G, typ}$	16.5	nC
$Q_{RR, typ}$	63	nC

Applications

- High efficiency power supplies
- Telecom and datacom
- Automotive
- Servo motors

Schematic Symbol

Cascode Device Structure
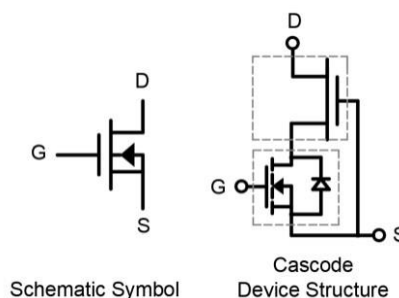
Packaging

Part Number	Package	Packaging	Base QTY
RX65T125PS2A	3 Lead TO-220	Tube	50

Maximum ratings, at T_C=25 ℃, unless otherwise specified

Symbol	Parameter		Limit Value	Unit
I_D	Continuous drain current @T_C=25℃		20	A
	Continuous drain current @T_C=100℃		13	A
I_{DM}	Pulsed drain current @T_C=25℃ (pulse width: 100us)		64	A
	Pulsed drain current @T_C=150℃ (pulse width: 100us)		47	A
V_{DSS}	Drain to source voltage (T_J = -55℃ to 150℃)		650	V
V_{TDSS}	Transient drain to source voltage [a]		800	V
V_{GSS}	Gate to source voltage		±20	V
P_D	Maximum power dissipation @T_C=25℃		100	W
T_C	Operating temperature	Case	-55 to 150	℃
T_J		Junction	-55 to 150	℃
T_S	Storage temperature		-55 to 150	℃
T_{CSOLD}	Soldering peak temperature		260	℃

Thermal Resistance

Symbol	Parameter	Typical	Unit
$R_{\theta JC}$	Junction-to-case	1.25	℃/W
$R_{\theta JA}$	Junction-to-ambient [b]	50	℃/W

Notes:

a. Off-state spike duty cycle < 0.01, spike duration < 2us

b. Device on one layer epoxy PCB for drain connection (vertical and without air stream cooling, with 6cm^2 copper area and 70μm thickness)

Electrical Parameters, at T_J=25 ℃, unless otherwise specified

| Symbol	Min	Typ	Max	Unit	Test Conditions
Forward Characteristics					
$V_{DSS-MAX}$	650	-	-	V	V_{GS}=0V
BV_{DSS}	-	1000	-		V_{GS}=0V, I_{DSS}=250μA
$V_{GS(th)}$	3	4	5	V	V_{DS}=V_{GS}, I_D=500μA
$\triangle V_{GS(th)}/T_J$	-	-10.7	-	mV/℃	
$R_{DS(on)}$ [c]	-	120	150	mΩ	V_{GS}=12V, I_D=4A, T_J=25℃
	-	240	-		V_{GS}=12V, I_D=4A, T_J=150℃
I_{DSS}	-	8	20	μA	V_{DS}=700V, V_{GS}=0V, T_J=25℃
	-	50	-	μA	V_{DS}=700V, V_{GS}=0V, T_J=150℃
I_{GSS}	-	-	150	nA	V_{GS}=20V
	-	-	-150	nA	V_{GS}=-20V
C_{ISS}	-	635	-	pF	VGS=0V, VDS=400V, f=1MHz
C_{OSS}	-	57	-	pF	
C_{RSS}	-	2.5	-	pF	
$C_{O(er)}$	-	83	-	pF	V_{GS}=0V, V_{DS}=0 - 400V
$C_{O(tr)}$	-	158	-	pF	
Q_{oss}	-	63	-	nC	
Q_G	-	16.5	-	nC	V_{DS}=400V, V_{GS}=0 - 12V, I_D=13A
Q_{GS}	-	5	-		
Q_{GD}	-	5.7	-		
$t_{D(on)}$	-	30	-	ns	V_{DS}=400V, V_{GS}=0 - 12V, I_D=10A, R_G=47Ω
t_R	-	16	-		
$t_{D(off)}$	-	80	-		
t_F	-	10	-		
Reverse Characteristics					
V_{SD}	-	1.3	-	V	V_{GS}=0V, I_S=6.5A, T_J=25℃
	-	2.1	-		V_{GS}=0V, I_S=13A, T_J=25℃
	-	2.9	-		V_{GS}=0V, I_S=13A, T_J=150℃
t_{RR}	-	27	-	ns	I_S=13A, V_{GS}=0V, d_i/d_t=1000A/us, V_{DD}=400V
Q_{RR}	-	63	-	nC	

Notes:

c. Dynamic on-resistance; see Figure 18 and 19 for test circuit and configurations

Circuit Implementation

Mostly used in half bridge and full bridge topology
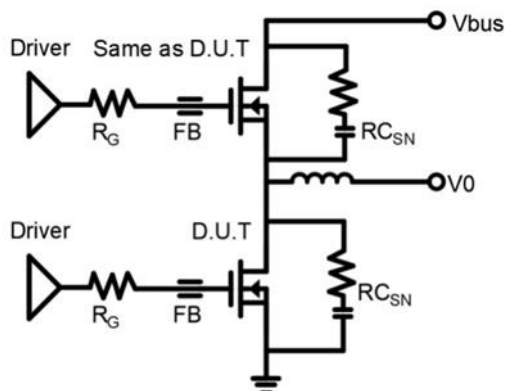
Recommended Half-bridge Circuit

Recommended gate drive: (0 V, 12 V) with $R_{G(tot)}$ = 40 Ω, where $R_{G(tot)}$ = R_G + R_{driver}

Gate Ferrite Bead (FB)	Gate Resistance (R_G)	RC Snubber (RC_{SN})
MPZ1608S471ATA00	33 Ω	69 pF + 15 Ω

Notes:

d. RC_{SN} should be placed as close as possible to the drain pin

e. The layout and wiring of the drive circuit should be as short as possible

Typical Characteristics, at T_C=25 ℃, unless otherwise specified

Figure 1. Typical Output Characteristics T_J=25℃

Parameter: V_{GS}

Figure 2. Typical Output Characteristics T_J=150℃

Parameter: V_{GS}

Figure 3. Typical Transfer Characteristics

V_{DS}=10V, Parameter: T_J

Figure 4. $V_{GS(th)}$ Vs Temperature Characteristics

I_D=500uA

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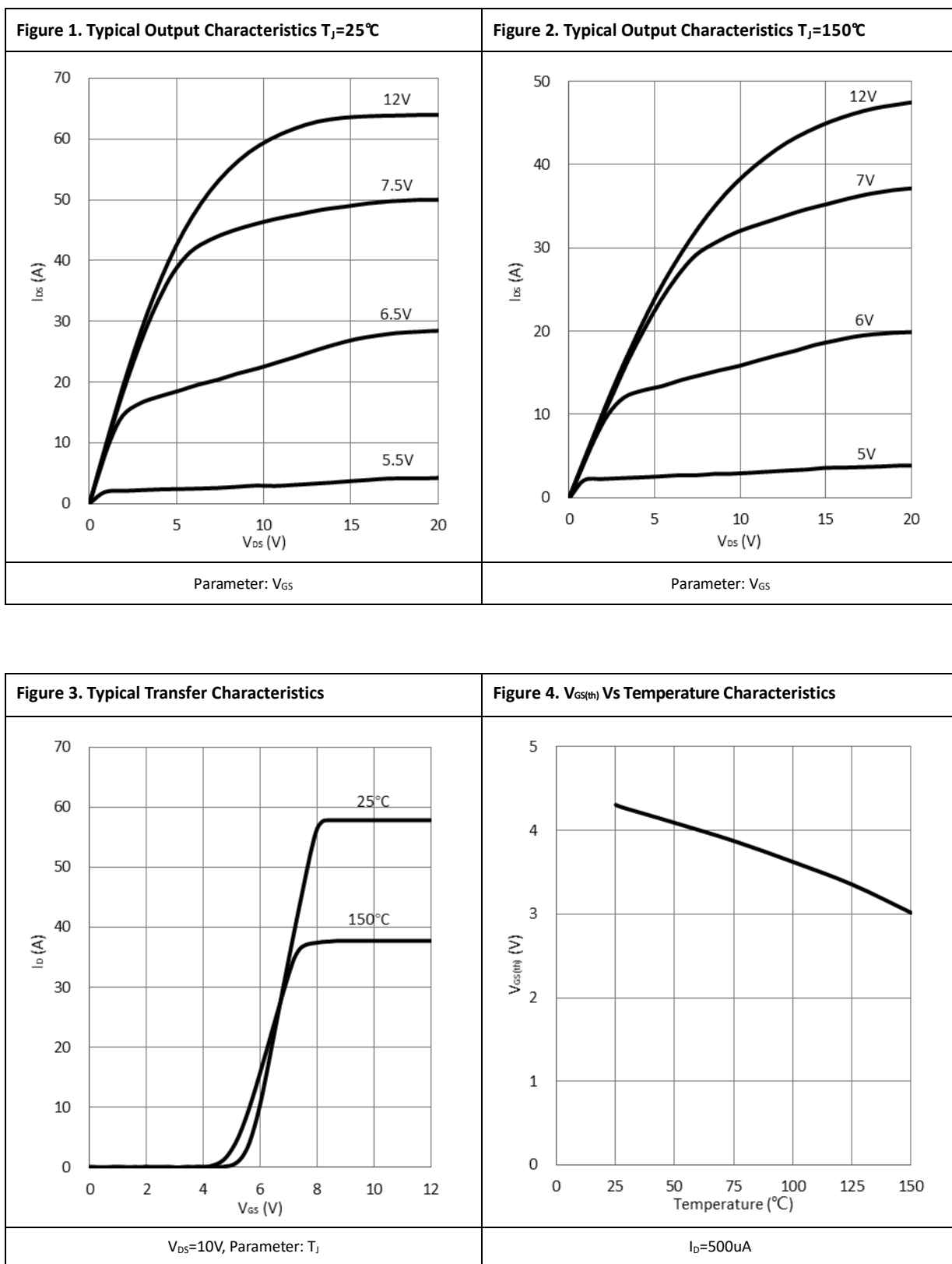
Figure 5. Normalized On-resistance	Figure 6. Typical Capacitance
I_D=4A, V_{GS}=12V	V_{GS}=0V, f=1MHz
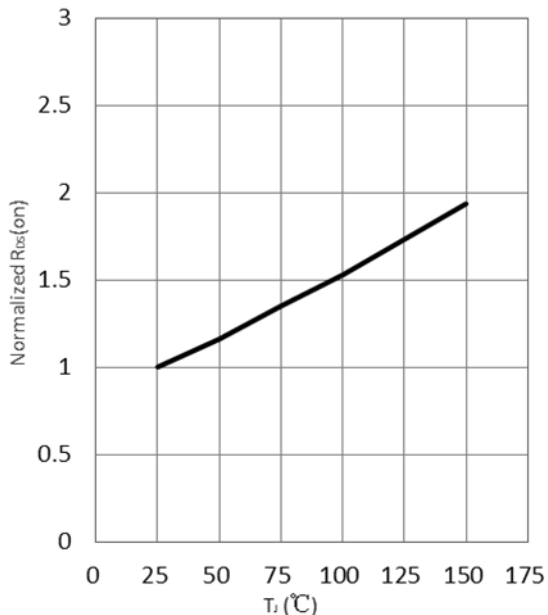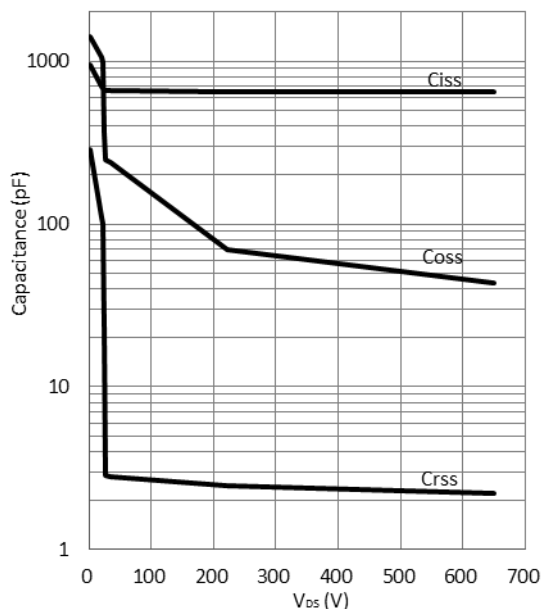
Figure 7. Typical Coss Stored Energy	Figure 8. Typical Qoss
V_{GS}=0V, f=1MHz	V_{GS}=0V, f=1MHz
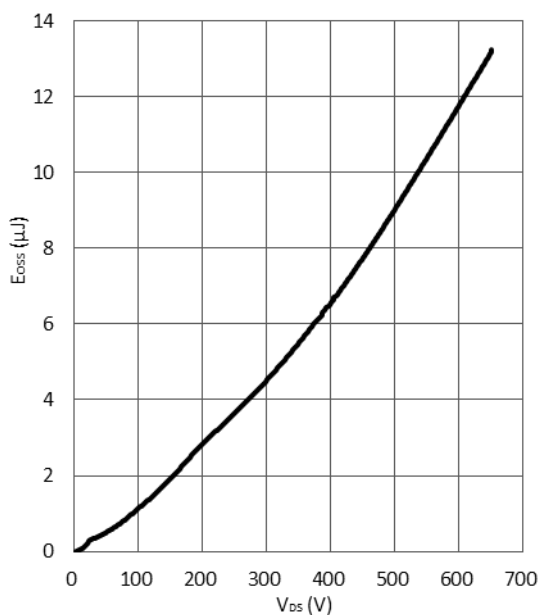
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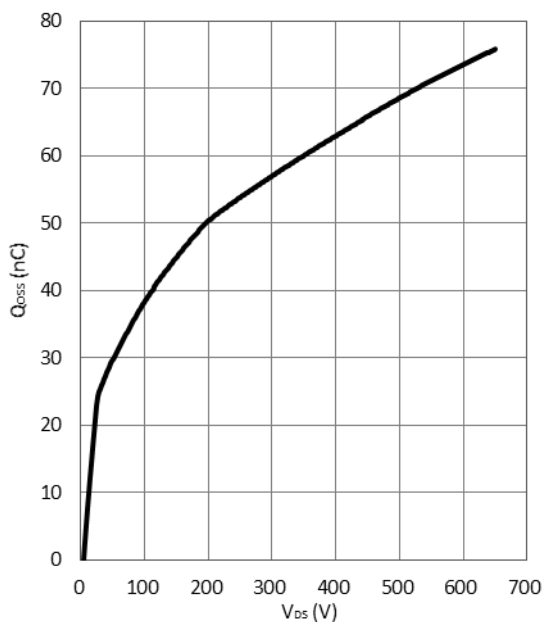
Figure 9. Forward Characteristic of Rev. Diode	Figure 10. Typical Gate Charge
Is=f(V_{SD}), Parameter T_J	I_{DS}=13A, V_{DS}=400V
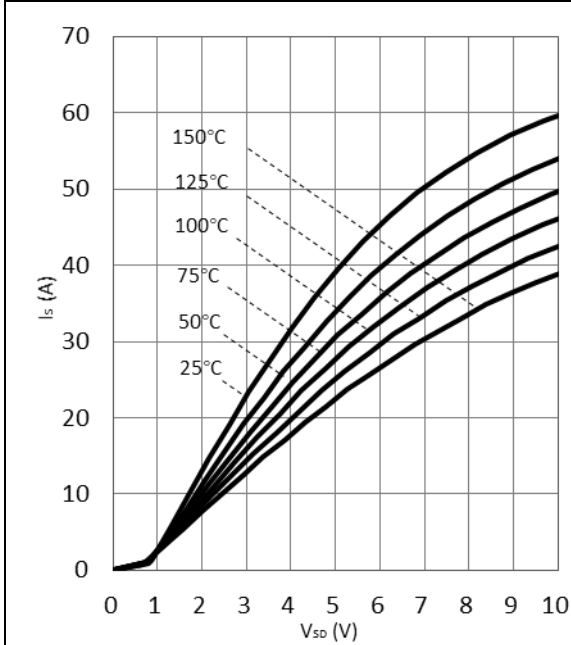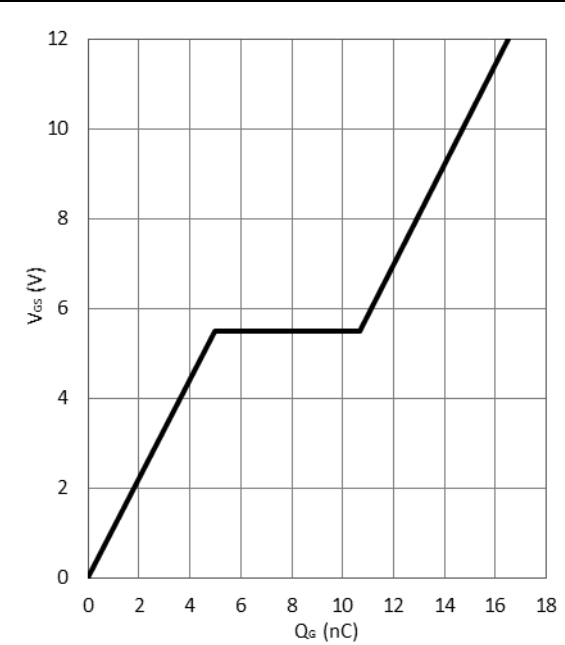
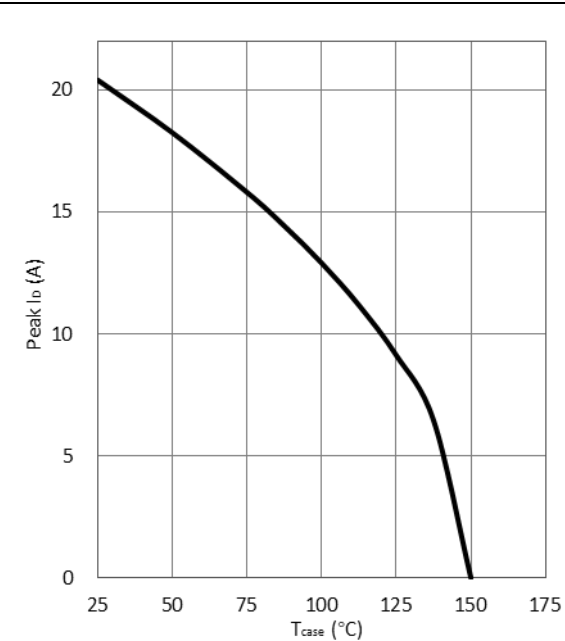| Figure 11. Power Dissipation	Figure 12. Current Derating
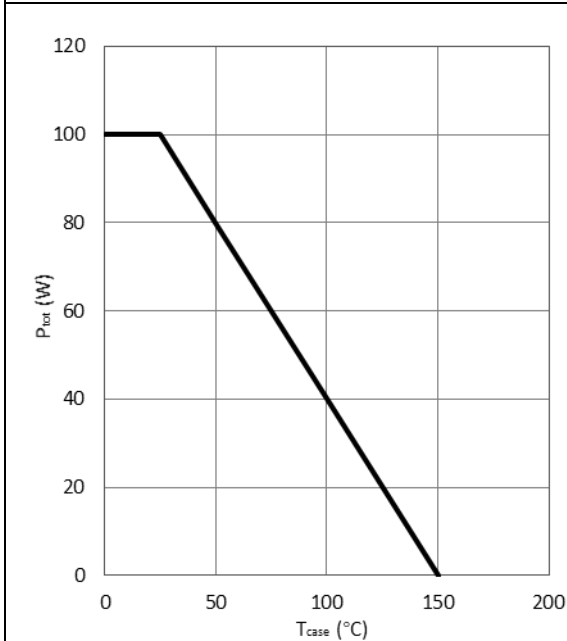
Figure 13. Transient Thermal Resistance	Figure 14. Safe Operating Area $T_C=25℃$
	calculated based on thermal limit
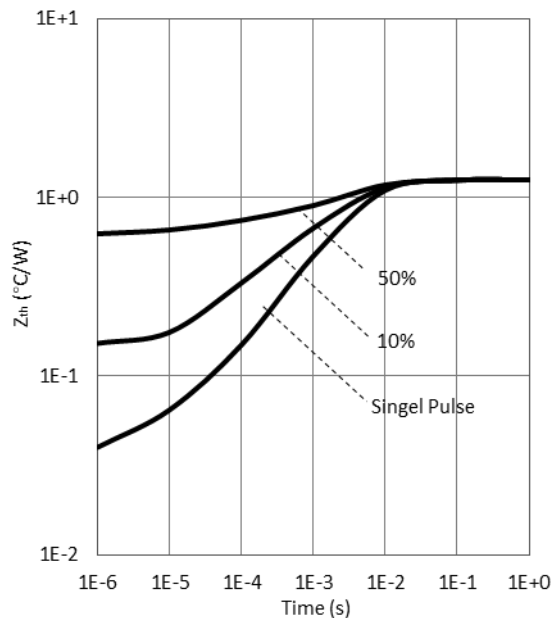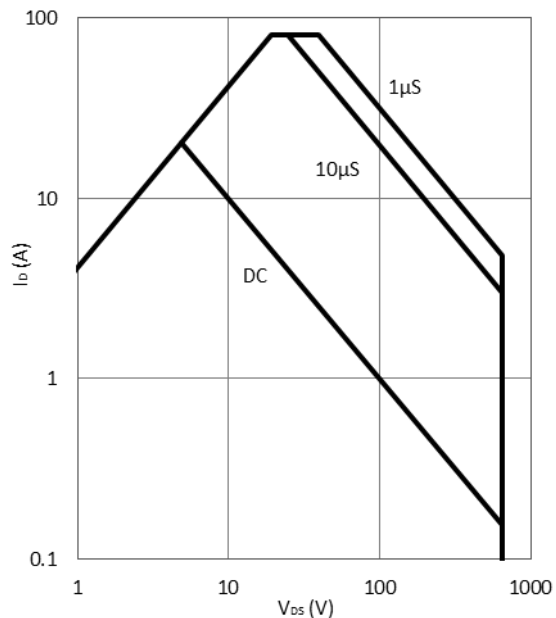
Figure 15. Safe Operating Area $T_C=80℃$
calculated based on thermal limit

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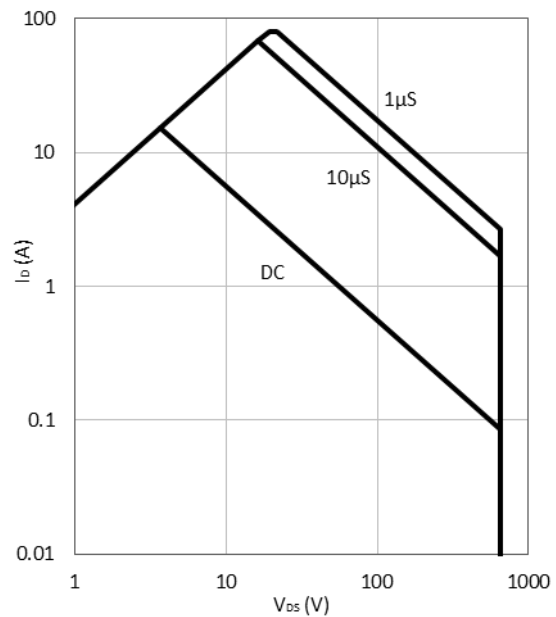
Test Circuits and Waveforms

Figure 16. Switching Time Test Circuit	Figure 17. Switching Time Waveform
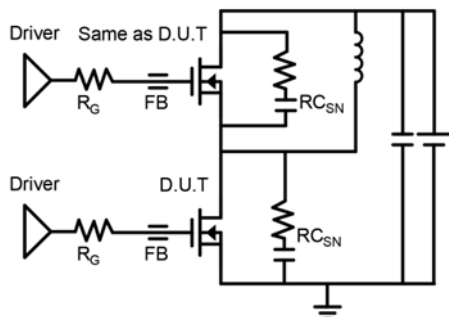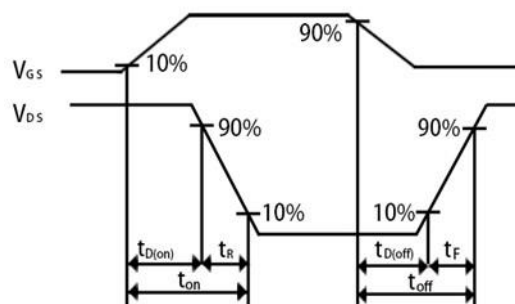
Figure 18. Dynamic $R_{DS(on)}$ Test Circuit	Figure 19. Dynamic $R_{DS(on)}$ Waveform
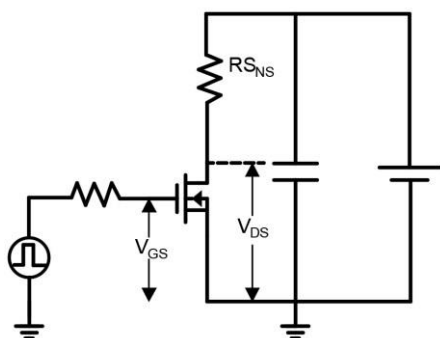
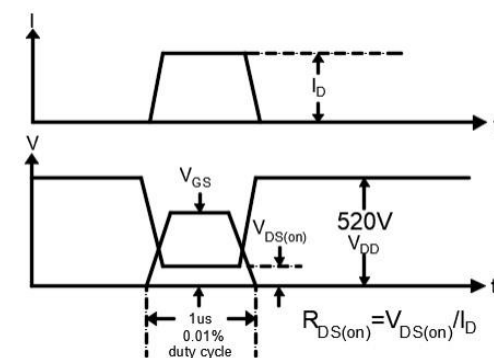| Figure 20. Diode Characteristic Test Circuits	Figure 21. Diode Recovery Waveform

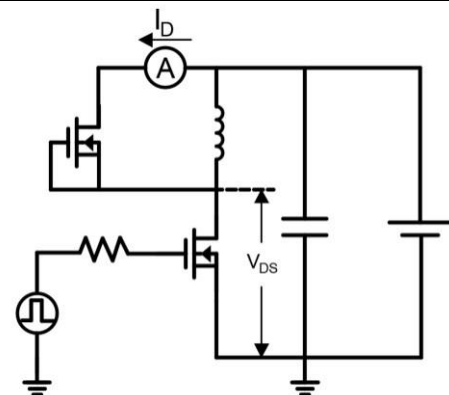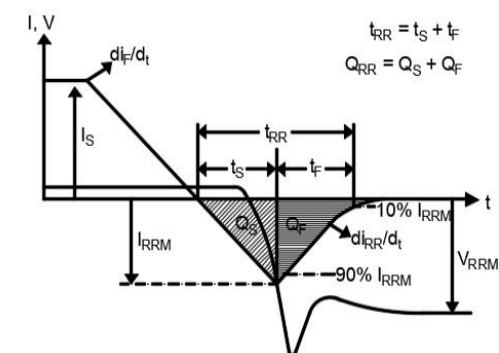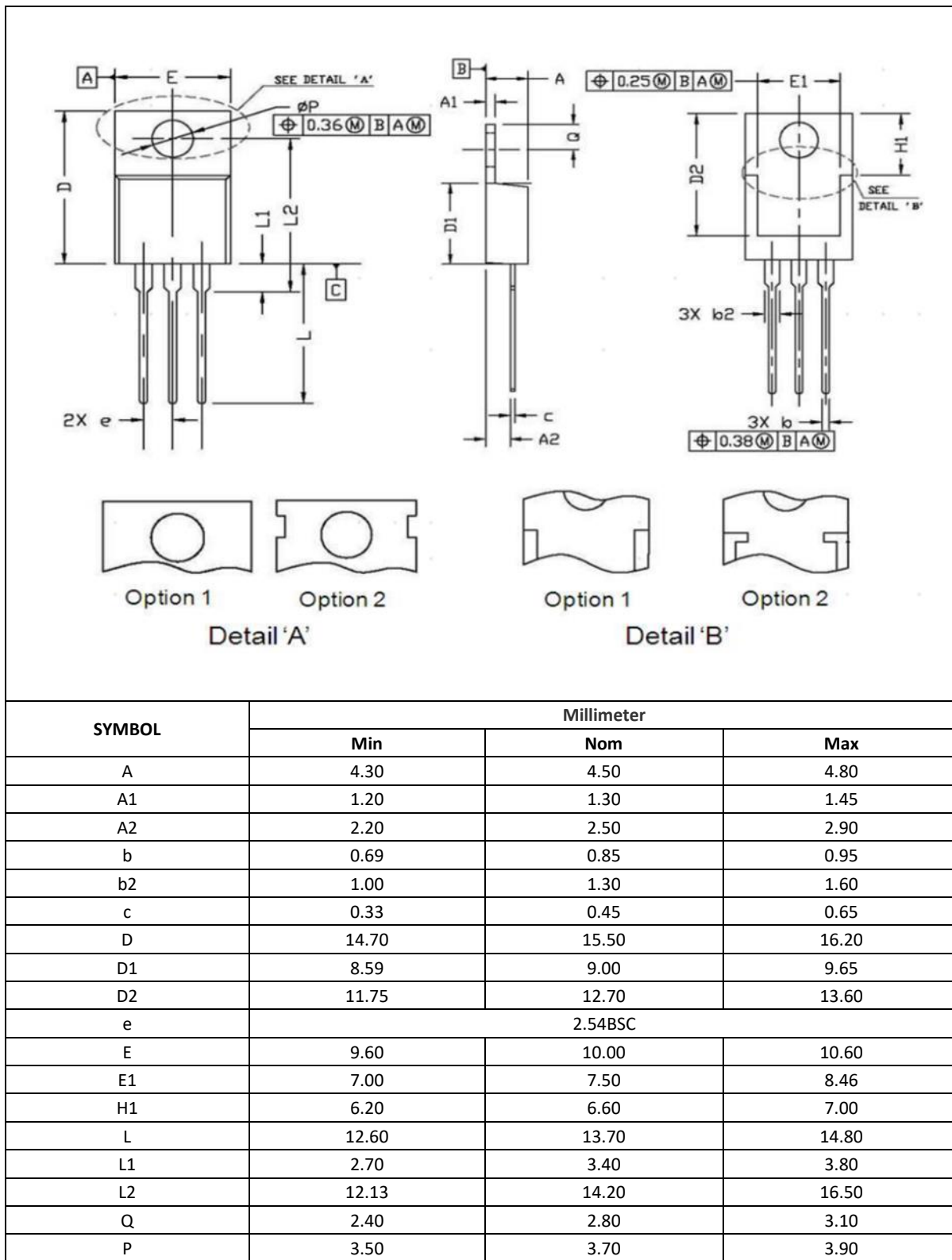**Design Considerations**

Fast switching GaN device can reduce power conversion losses, and thus enable high frequency operations. Certain PCB design rules and instructions, however, need to be followed to take full advantages of fast switching GaN devices.

Before evaluating Runxin Micro's GaN devices, please refer to the table below which provides some practical rules that should be followed during the evaluation.

When Evaluating Runxin Micro's GaN Devices:

DO	DO NOT
Make sure the traces are as short as possible for both drive and power loops to minimize parasitic inductance	Using Runxin Micro's devices in GDS board layouts
Use the test tool with the shortest inductive loop, and make sure test points should be placed close enough	Use differential mode probe or probe ground clip with long wires
Minimize the lead length of DFN 8*8mm packages when installing them to PCB	Use long traces in drive circuit, or long lead length of the devices

Package Outline

SYMBOL	Millimeter		
	Min	Nom	Max
A	4.30	4.50	4.80
A1	1.20	1.30	1.45
A2	2.20	2.50	2.90
b	0.69	0.85	0.95
b2	1.00	1.30	1.60
c	0.33	0.45	0.65
D	14.70	15.50	16.20
D1	8.59	9.00	9.65
D2	11.75	12.70	13.60
e	2.54BSC		
E	9.60	10.00	10.60
E1	7.00	7.50	8.46
H1	6.20	6.60	7.00
L	12.60	13.70	14.80
L1	2.70	3.40	3.80
L2	12.13	14.20	16.50
Q	2.40	2.80	3.10
P	3.50	3.70	3.90

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RX65T125PS2A

Tube Information   **Dimensions are shown in millimeters**

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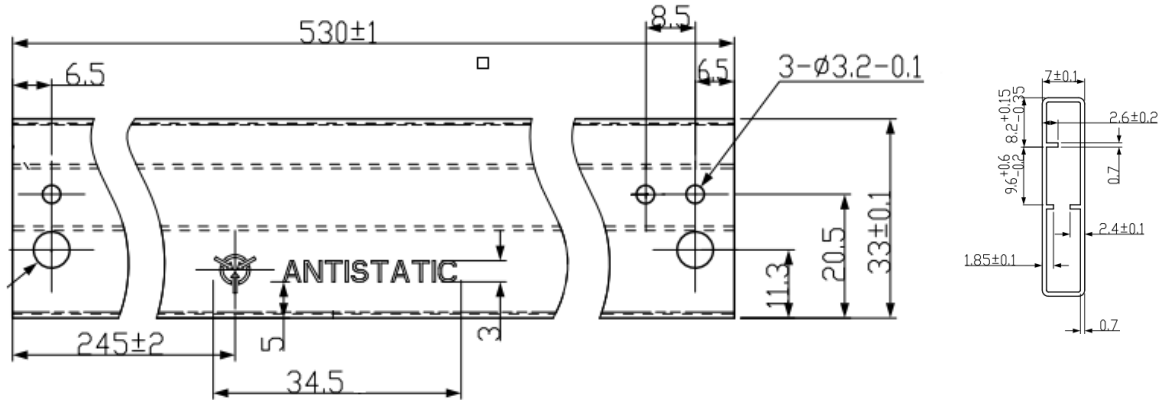
Revision History

Version	Date	Change(s)
1.0	2023/01/16	Release formal datasheet
1.1	2023/05/17	Revise C_{ISS}, C_{OSS}, C_{RSS}, $C_{o(er)}$, $C_{o(tr)}$, SOA
1.2	2023/08/10	Revise C_{ISS}, C_{OSS}, C_{RSS}, $C_{o(er)}$, $C_{o(tr)}$
1.3	2023/11/24	Revise Qg, Output, Transfer, Is, Outline, Disclaimer
1.4	2024/01/16	Revise I_D, Q_{oss}, Q_{RR}, t_{RR}, $\triangle V_{GS(th)}/T_J$, Figure 4/12/13/14/15
1.5	2024/07/18	Revise $\triangle V_{GS(th)}/T_J$, I_{DSS}, C_{ISS}, C_{RSS}, $C_{o(tr)}$, Q_G, $t_{D(on)}$, $t_{D(off)}$, Figure 6/8/10

Disclaimer

Unless otherwise specified in the datasheet, the product is designed and qualified as a standard commercial product and is not intended for use in applications that require extraordinary levels of quality and reliability, such as automotive, aviation/aerospace and life-support devices or systems.

Any and all semiconductor products have certain probability to fail or malfunction, which may result in personal injury, death or property damage. Customer are solely responsible for providing adequate safe measures when design their systems.